JADAVPUR UNIVERSITY

IC DESIGN AND FABRICATION CENTRE

SUMMER TRAINING ON MICRO-ELECTRONICS TECHNOLOGY AND VLSI DESIGN

PRACTICAL REPORT
ON
EDA (DIGITAL & ANALOG) LAB

BY~

INSTITUTE OF ENGINEERING AND MANAGEMENT, KOLKATA(IEM)

GROUP – 1

TEAM MEMBERS

NAMES	STREAM/ YEAR
SOMAK KUMAR	ECE/ 3rd Year
ABHISHEK ANAND	ECE/ 3rd Year
SAYANTAN SARKAR	ECE/ 3rd Year
APARAJITA ROY	ECE/ 3rd Year
SOURAJIT NAYAK	ECE/ 3rd Year
LAWAZ ISLAM	ECE/ 3rd Year
DEBAYAN SENGUPTA	ECE/ 3rd Year
VISHWAVIJAY SINGH	ECE/ 3rd Year

ACKNOWLEDGEMENT

We received a lot of information and advice from some well-respected people who deserve our gratitude for helping us with our lab studies. As a result, I'd want to express our heartfelt gratitude to everyone who has helped us along the way, both directly and indirectly. First and foremost, I want to express my gratitude to respected Professors, who introduced us to the work approach and whose sincere advice, inspiration, and participation opened the path for the effective completion of our report. I'd like to express my gratitude to him in particular for sharing the ups and downs of the development process and putting up with the inconvenience. I'd also like to offer my heartfelt gratitude to all the members of Jadavpur University for their cooperation, recommendations, and unwavering support. Most significantly, by allowing us the access to the IC centre and its technologies to us, have provided valuable feedback on this proposal, inspiring us to prepare ourselves for a better future. Last but not the least, I appreciate everyone's assistance in performing our lab experiments.

EDA : DIGITAL CONTENTS

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INTRODUCTION

Electronic design automation (EDA), also referred to as electronic computer-aided design (ECAD), is a category of software tools for designing electronic systems such as integrated circuits and printed circuit boards. The tools work together in a design flow that chip designers use to design and analyze entire semiconductor chips. There is simply no way to manage this level of complexity without sophisticated automation, and EDA provides this critical technology. Without it , it would be impossible to design and manufacture today's semiconductor devices. Since a modern semiconductor chip can have billions of components, EDA tools are essential for their design; this article in particular describes EDA specifically with respect to integrated circuits (ICs).

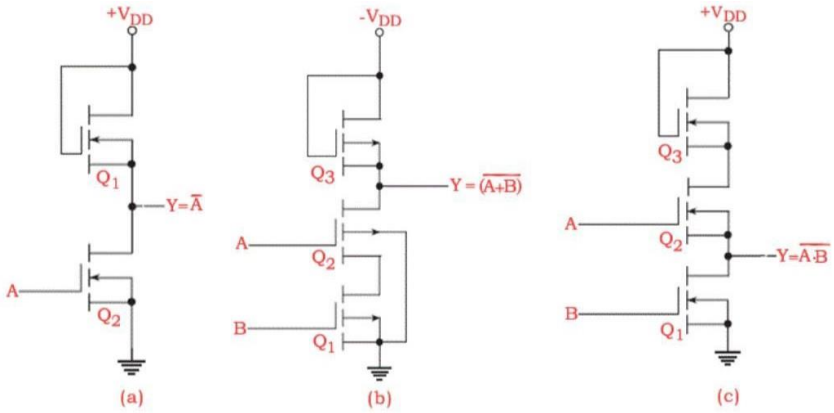
Here we are going to explore EDA and the different characteristics with the help of the below mentioned software –

- S-edit
- T-spice
- W-edit

NMOS LOGIC FAMILY

The NMOS logic family uses N-channel MOSFETS. N-channel MOS devices require a smaller chip area per transistor compared with P-channel devices, with the result that NMOS logic offers a higher density. Also, owing to the greater mobility of the charge carriers in N-channel devices, the NMOS logic family offers higher speed too.

It Is for this reason that most of the MOS memory devices and microprocessors employ NMOS logic or some variation of it such as VMOS, DMOS and HMOS. VMOS, DMOS and HMOS are only structural variations of NMOS, aimed at further reducing the propagation delay. Figures (a), (b) and (c) respectively show an inverter, a two-input NOR and a two-input NAND using NMOS logic. The logic circuits are self-explanatory.



(a) NMOS logic circuit inverter, (b) NMOS logic two-input NOR and
(c) NMOS logic two-input

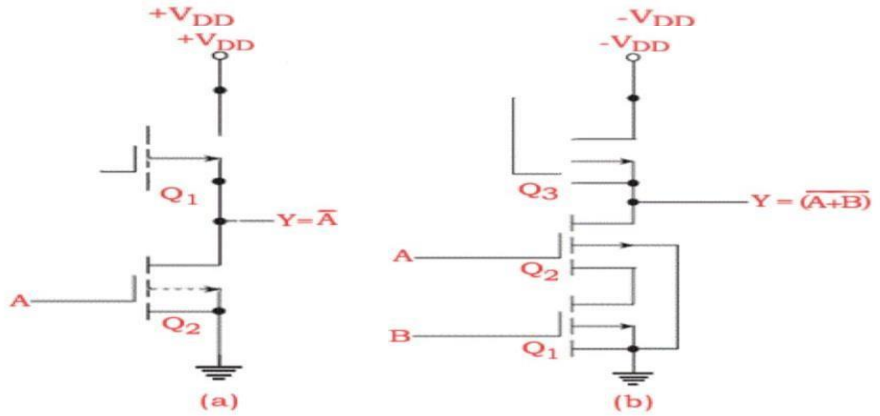
PMOS LOGIC FAMILY

The PMOS logic family uses P-channel MOSFETS. Figure (a) shows aninverter circuit using PMOS logic (not to be confused with a power inverter). MOSFET Q1 acts as an active load for the MOSFET switch Q2. For the circuit shown,

GND and −VDD respectively represent a logic ‘1’ and a logic ‘0’ for a positive logic system. When the input is grounded (i.e. logic ‘1’), Q2

remains in cut-off and −VDD appears at the output through the conducting Q1. When the input is at −VDD or near −VDD, Q2 conducts and the output goes to near-zero potential (i.e. logic '1'). Figure (b) shows a PMOS logic based two-input NOR gate. In the logicarrangement of Fig.(b), the output goes to logic '1' state (i.e. ground potential) only when both Q1 and Q2 are conducting.

This is possible only when both the inputs are in logic '0' state. For all other possible input combinations, the output is in logic '0' state, because, with either Q1 or Q2 nonconducting, the output is nearly −VDD through the conducting Q3. The circuit of Fig.(b) thus behaveslike a two-input NOR gate in positive logic.



(a) PMOS logic inverter and (b) PMOS logic two-input NOR

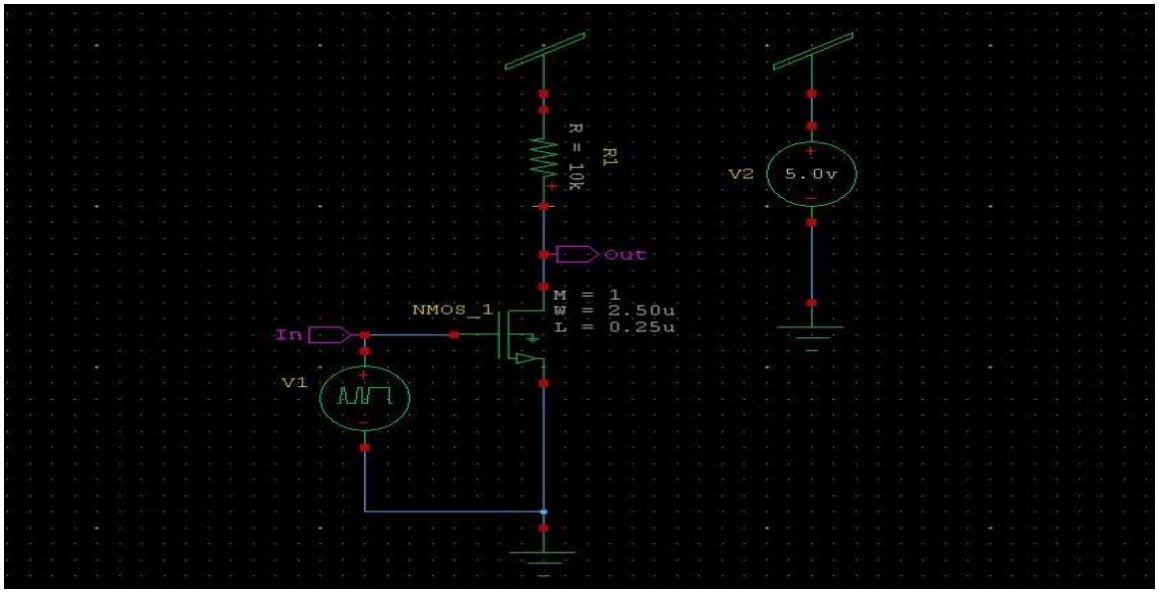
CMOS LOGIC FAMILY

CMOS logic family is a group of logic circuits, built with complementary MOS devices. All the logic gates that are built with MOSFET devices will come under MOS logic family. MOS Logic familycan be classified into three categories. They are

1. logic family – built with N-channel Metal oxide semiconductor FET (MOSFET)
2. logic family – built with P-channel Metal oxide semiconductor FET (MOSFET)
3. CMOS logic family – built with both N-channel and P-channel Metal oxidesemiconductor FET (MOSFET)

DESIGN OF RESISTIVE LOAD INVERTER

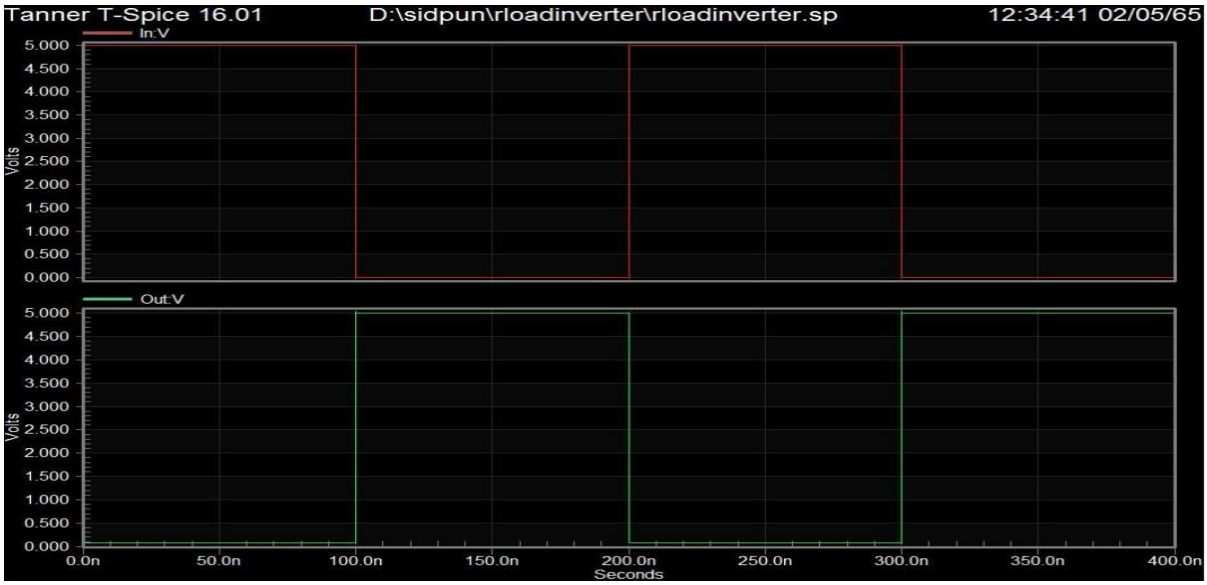
CIRCUIT DIAGRAM:



T-Spice Code:

```
RR1 Out Vdd R=10k
MNMOS_1 Out In Gnd 0 NMOS W=450n L=150n AS=2.25p PS=6.8u AD=2.25u PD=6.8u
VV2 Vdd Gnd DC 5
V1 In Gnd BIT({1010} lt=100n on=5 off=0 rt=0.1n ft=0.1n)
.include “C:\Users\user1\Desktop\dual.md”
.tran 1n 400n
.print V(In) V(Out)
.end
```

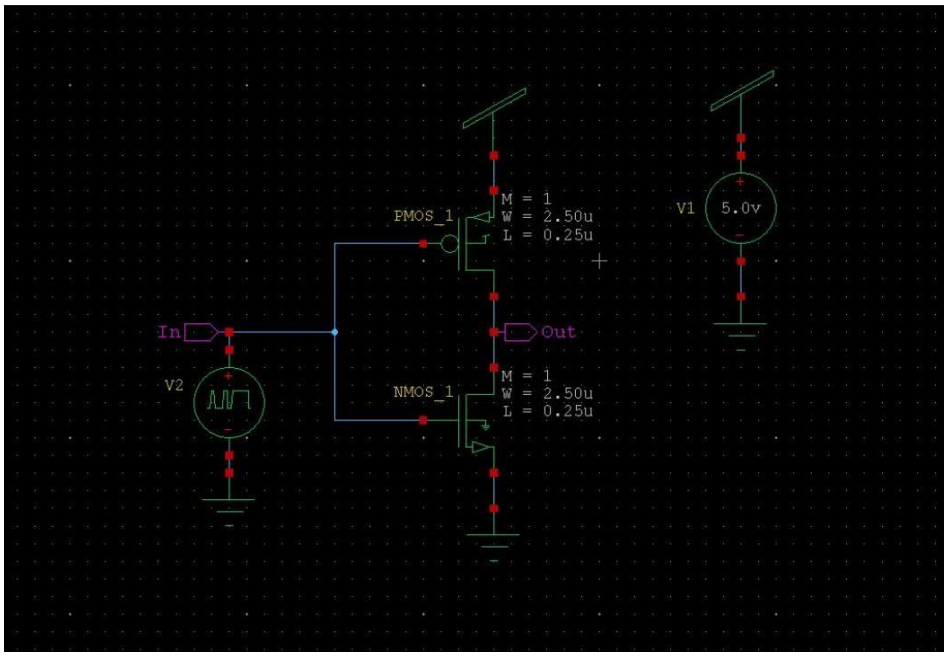
OUTPUT WAVEFORM:



Design of CMOS Invertor

A CMOS (Complementary Metal-oxide Semiconductor) inverter is a device that produces logic functions and is the primary component of all integrated circuits. A CMOS inverter is a field-effect transistor that is composed of a metal gate that lies on top of an insulating layer of oxygen, which lies on top of a semiconductor. CMOS inverters are found in most electronic devices and are responsible for producing data within small circuits.

Circuit Diagram:



T-Spice Code:

```
MNMOS_1 Out In Gnd 0 NMOS W=450n L=150n AS=2.25p PS=6.8u AD=2.25u PD=6.8u
MPMOS_1 Out In Vdd Vdd PMOS W=900n L=150n AS=2.25p PS=6.8u AD=2.25u PD=6.8u
VV1 Vdd Gnd 1 V1 In Gnd BIT({1010} lt=100n on=5 off=0 rt=0.1n ft=0.1n)

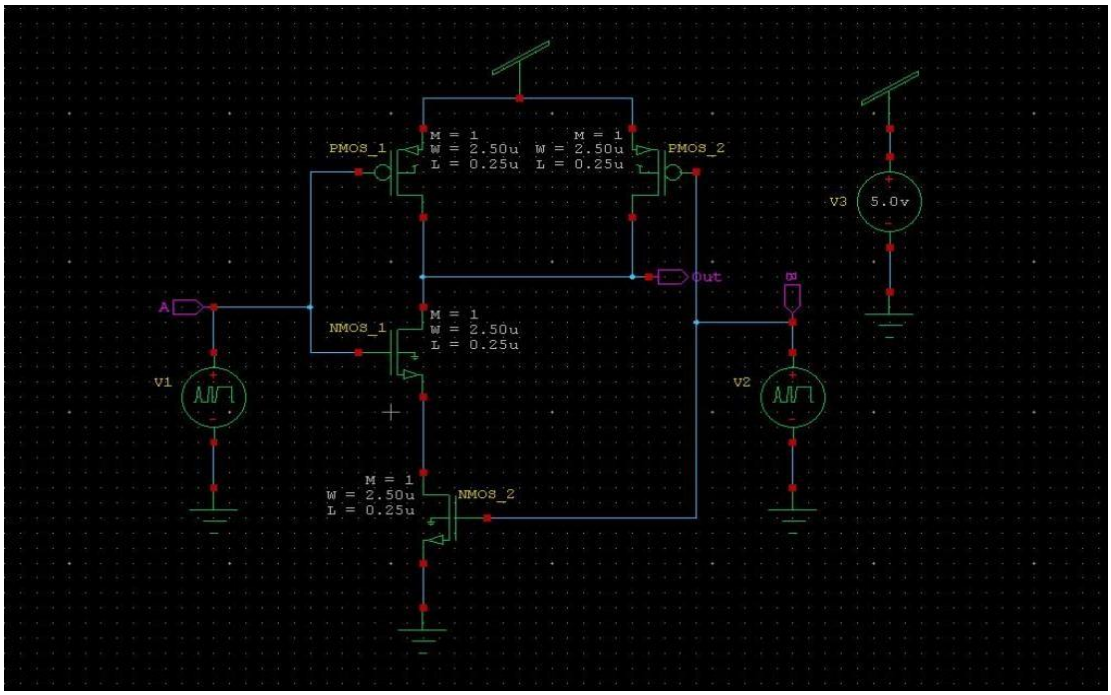
.include “C:\Users\user1\Desktop\dual.md”
.tran 1n 400n
.print V(In) V(Out)
.end
```

OUTPUT WAVEFORM:



Design of CMOS NAND Gate

Circuit Diagram:



T-Spice Code:

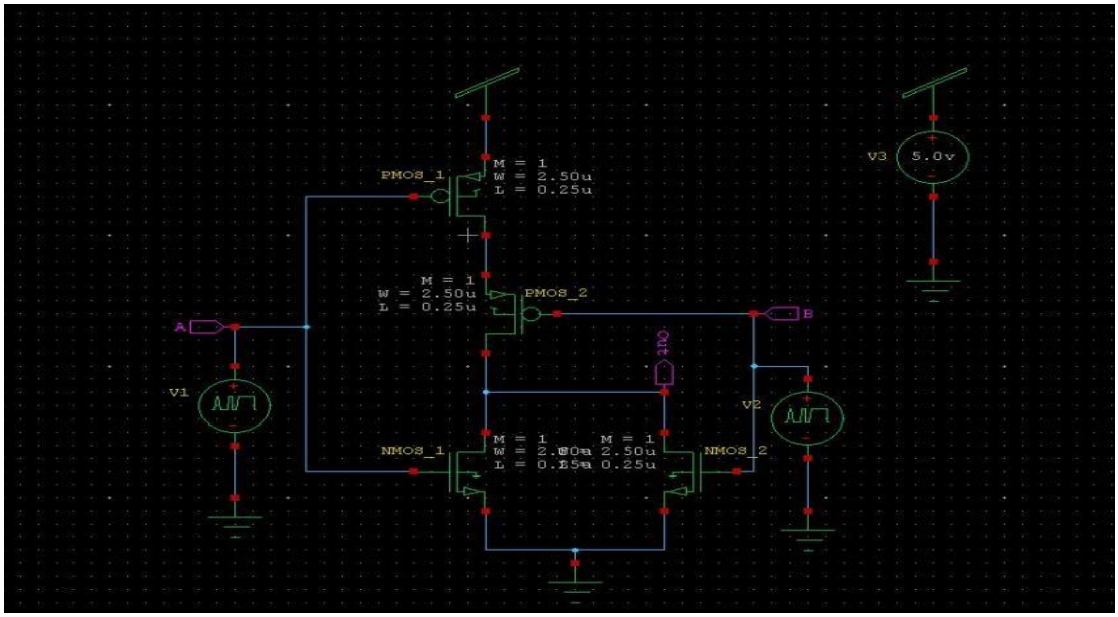
```
MNMOS_1 Out A N_1 0 NMOS =450n L=150n AS=2.25p PS=6.8u AD=2.25u PD=6.8u
MNMOS_2 N_1 B Gnd 0 NMOS =450n L=150n AS=2.25p PS=6.8u AD=2.25u PD=6.8u
MPMOS_1 Out A Vdd Vdd PMOS W=900n L=150n AS=2.25p PS=6.8u AD=2.25uPD=6.8u
MPMOS_2 Out B Vdd Vdd PMOS W=900n L=150n AS=2.25p PS=6.8u AD=2.25uPD=6.8u
VV3 Vdd Gnd DC 5
V1 A Gnd BIT({0011} lt=100n on=5 off=0 rt=0.1n ft=0.1n)
V2 B Gnd BIT({0101} lt=100n on=5 off=0 rt=0.1n ft=0.1n)
.include “C:\Users\user1\Desktop\dual.md”
 .tran 1n 400n
.print V(A) V(B) V(Out)
.end
```

OUTPUT WAVEFORM:



Design of CMOS NOR Invertor

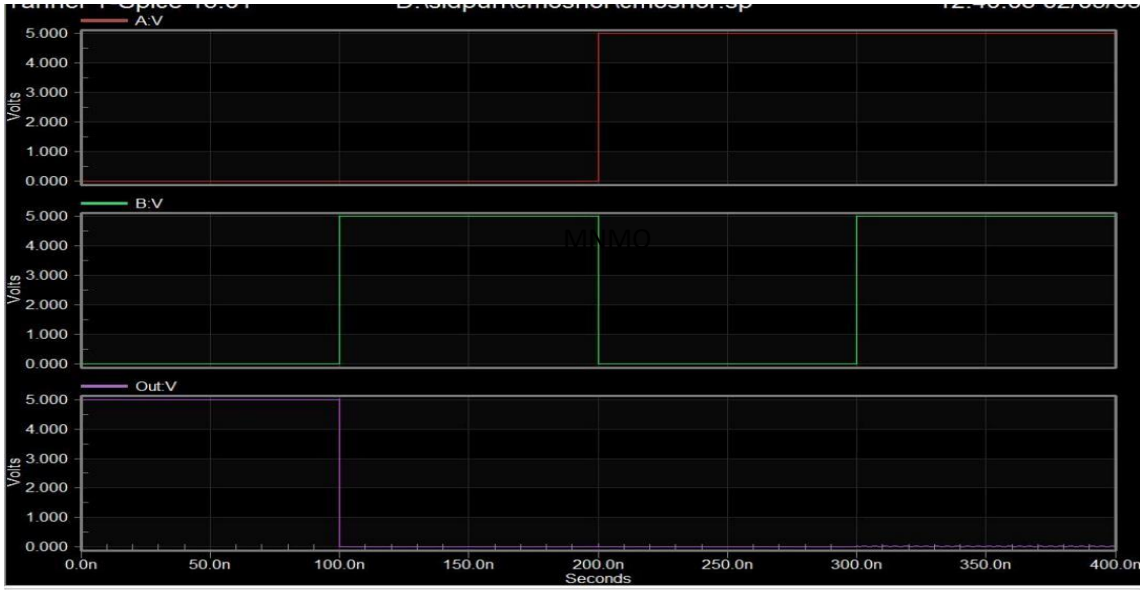
Circuit Diagram:



T-Spice Code:

```
MNMOS_1 Out A Gnd 0 NMOS =450n L=150n AS=2.25p PS=6.8u AD=2.25u PD=6.8u
MNMOS_2 Out B Gnd 0 NMOS =450n L=150n AS=2.25p PS=6.8u AD=2.25u PD=6.8u
MPMOS_1 N_1 A Vdd Vdd PMOS W=900n L=150n AS=2.25p PS=6.8u AD=2.25uPD=6.8u
MPMOS_2 Out B N_1 Vdd PMOS W=900n L=150n AS=2.25p PS=6.8u AD=2.25uPD=6.8u
VV3 Vdd Gnd DC 5
V1 A Gnd BIT({0011} lt=100n on=5 off=0 rt=0.1n ft=0.1n)
V2 B Gnd BIT({0101} lt=100n on=5 off=0 rt=0.1n ft=0.1n)
.include “C:\Users\user1\Desktop\dual.md”
 .tran 1n 400n
.print V(A) V(B) V(Out)
.end
```

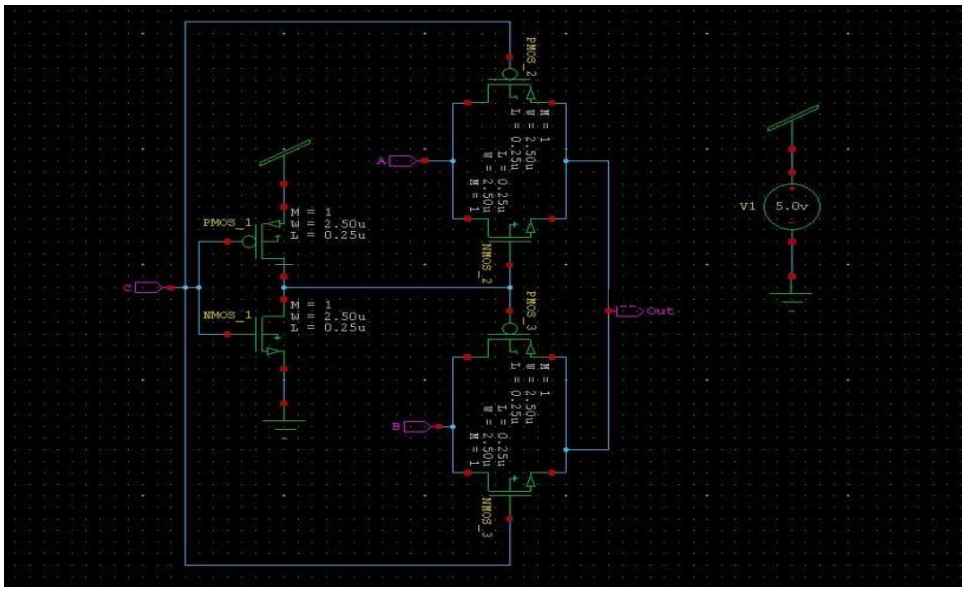
OUTPUT WAVEFORM:



Design of Transmission Gate Circuit

Transmission gates represent another class of logic circuits, which use Transmission gates as basic building block. A transmission gate consist of a PMOS and NMOS connected in parallel. A transmission gate, or analog switch, is defined as an electronic element that will selectively block or pass a signal level from the input to the output. This solid-state switch is comprised of a pMOS transistor and nMOS transistor. The control gates are biased in a complementary manner so that both transistors are either on or off.

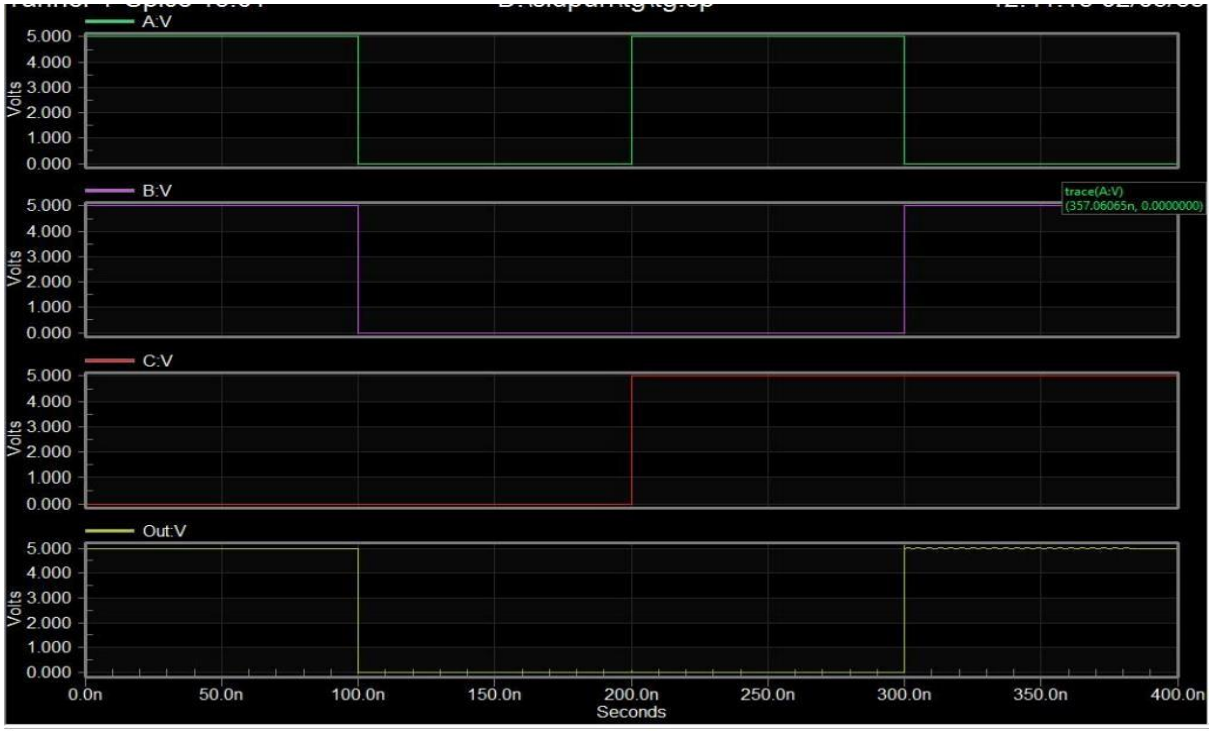
Circuit Diagram:



T-Spice Code:

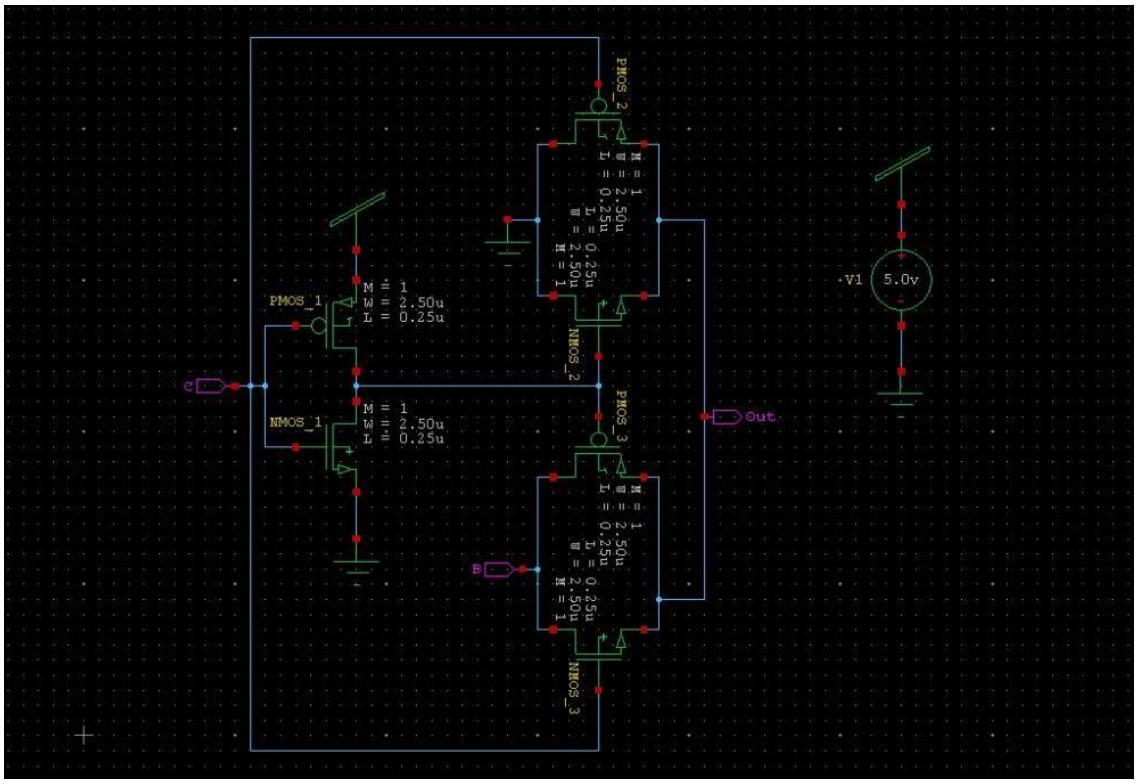
```
MNMOS_1 N_1 C Gnd 0 NMOS W=450n L=150n AS=2.25p PS=6.8u AD=2.25u PD=6.8u
MNMOS_2 A N_1 Out 0 NMOS W=450n L=150n AS=2.25p PS=6.8u AD=2.25u PD=6.8u
MNMOS_3 B C Out 0 NMOS W=450n L=150n AS=2.25p PS=6.8u AD=2.25u PD=6.8u
MPMOS_1 N_1 c Vdd Vdd PMOS W=900n L=150n AS=2.25p PS=6.8u AD=2.25uPD=6.8u
MPMOS_2 A C Out Vdd PMOS W=900n L=150n AS=2.25p PS=6.8u AD=2.25u PD=6.8u
MPMOS_3 B N_1 Out Vdd PMOS W=900n L=150n AS=2.25p PS=6.8u AD=2.25uPD=6.8u
VV1 Vdd Gnd DC 5
V3 A Gnd BIT({1010} lt=100n on=5 off=0 rt=0.1n ft=0.1n)
V2 C Gnd BIT({0011} lt=100n on=5 off=0 rt=0.1n ft=0.1n)
V1 B Gnd BIT({1001} lt=100n on=5 off=0 rt=0.1n ft=0.1n)
 .include “C:\Users\user1\Desktop\dual.md”
 .tran 1n 400n
 .print V(C) V(A) V(B) V(Out)
  .end
```

OUTPUT WAVEFORM:



Design of AND Gate using Transmission Gate Circuit

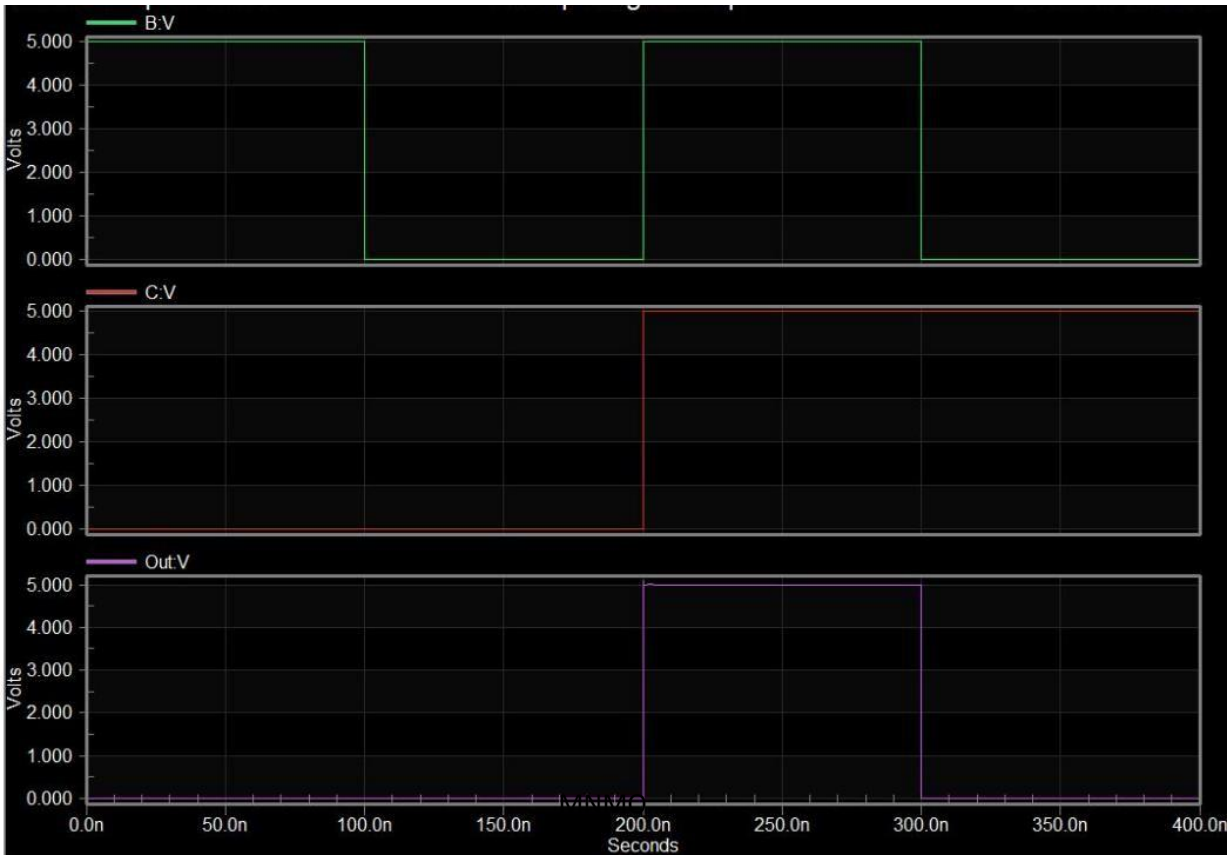
Circuit Diagram:



T-Spice Code:

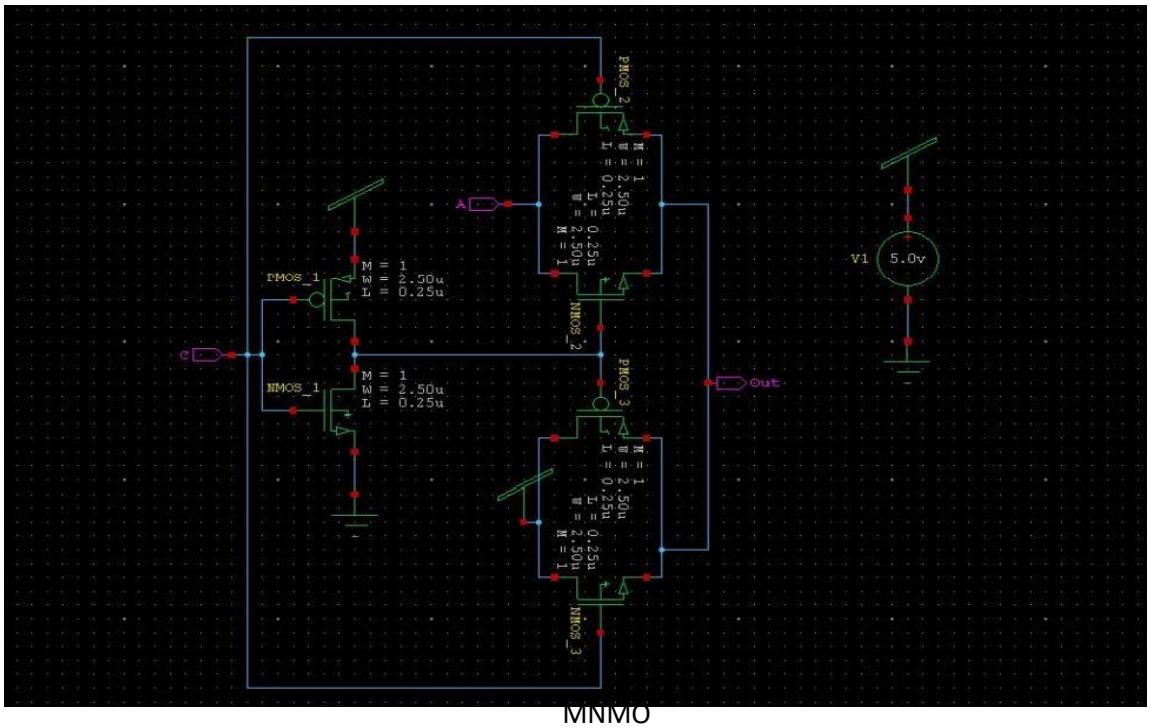
```
MNMOS_1 N_1 C Gnd 0 NMOS W=450n L=150n AS=2.25p PS=6.8u AD=2.25u PD=6.8u
MNMOS_2 Gnd N_1 Out 0 NMOS W=450n L=150n AS=2.25p PS=6.8u AD=2.25uPD=6.8u
MNMOS_3 B C Out 0 NMOS W=450n L=150n AS=2.25p PS=6.8u AD=2.25u PD=6.8u
MPMOS_1 N_1 C Vdd Vdd PMOS W=900n L=150n AS=2.25p PS=6.8u AD=2.25uPD=6.8u
MPMOS_2 Gnd C Out Vdd PMOS W=900n L=150n AS=2.25p PS=6.8u AD=2.25uPD=6.8u
MPMOS_3 B N_1 Out Vdd PMOS W=900n L=150n AS=2.25p PS=6.8u AD=2.25uPD=6.8u
VV1 Vdd Gnd DC 5
V2 C Gnd BIT({0011} lt=100n on=5 off=0 rt=0.1n ft=0.1n)
V4 B Gnd BIT({1010} lt=100n on=5 off=0 rt=0.1n ft=0.1n)
.include “C:\Users\user1\Desktop\dual.md”
 .tran 1n 400n
 .print V(C) V(B) V(Out)
 .end
```

OUTPUT WAVEFORM:



Design of OR Gate using Transmission Gate Circuit

Circuit Diagram:

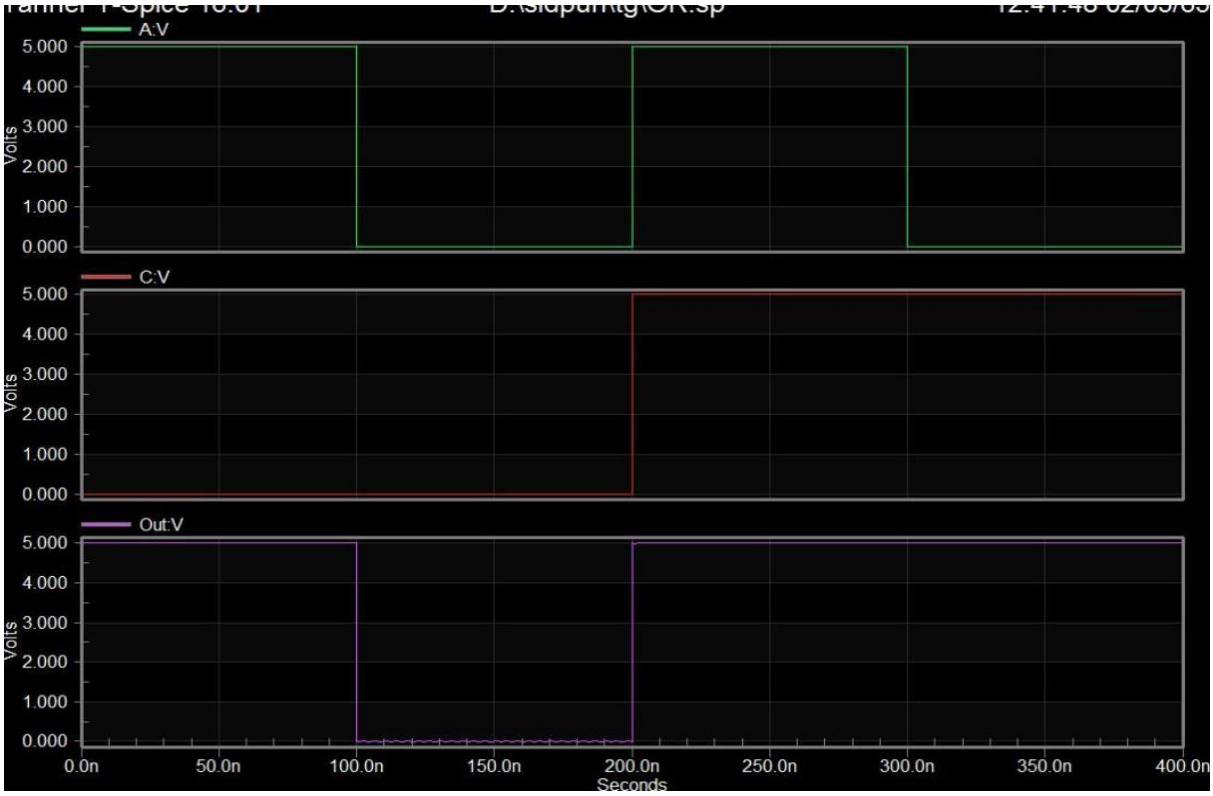


MNMO

T-Spice Code:

MNMOS_1 N_1 C Gnd 0 NMOS W=450n L=150n AS=2.25p PS=6.8u AD=2.25u PD=6.8u
MNMOS_2 A N_1 Out 0 NMOS W=450n L=150n AS=2.25p PS=6.8u AD=2.25u PD=6.8u
MNMOS_3 Vdd C Out 0 NMOS W=450n L=150n AS=2.25p PS=6.8u AD=2.25u PD=6.8u
MPMOS_1 N_1 C Vdd Vdd PMOS W=900n L=150n AS=2.25p PS=6.8u AD=2.25uPD=6.8u
MPMOS_2 A C Out Vdd PMOS W=900n L=150n AS=2.25p PS=6.8u AD=2.25u PD=6.8u
MPMOS_3 Vdd N_1 Out Vdd PMOS W=900n L=150n AS=2.25p PS=6.8u
AD=2.25uPD=6.8u
VV1 Vdd Gnd DC 5
V3 A Gnd BIT({1010} lt=100n on=5 off=0 rt=0.1n ft=0.1n)
V2 C Gnd BIT({0011} lt=100n on=5 off=0 rt=0.1n ft=0.1n)
.include “C:\Users\user1\Desktop\dual.md”
.tran 1n 400n
.print V(C) V(A) V(B) V(Out)
.end

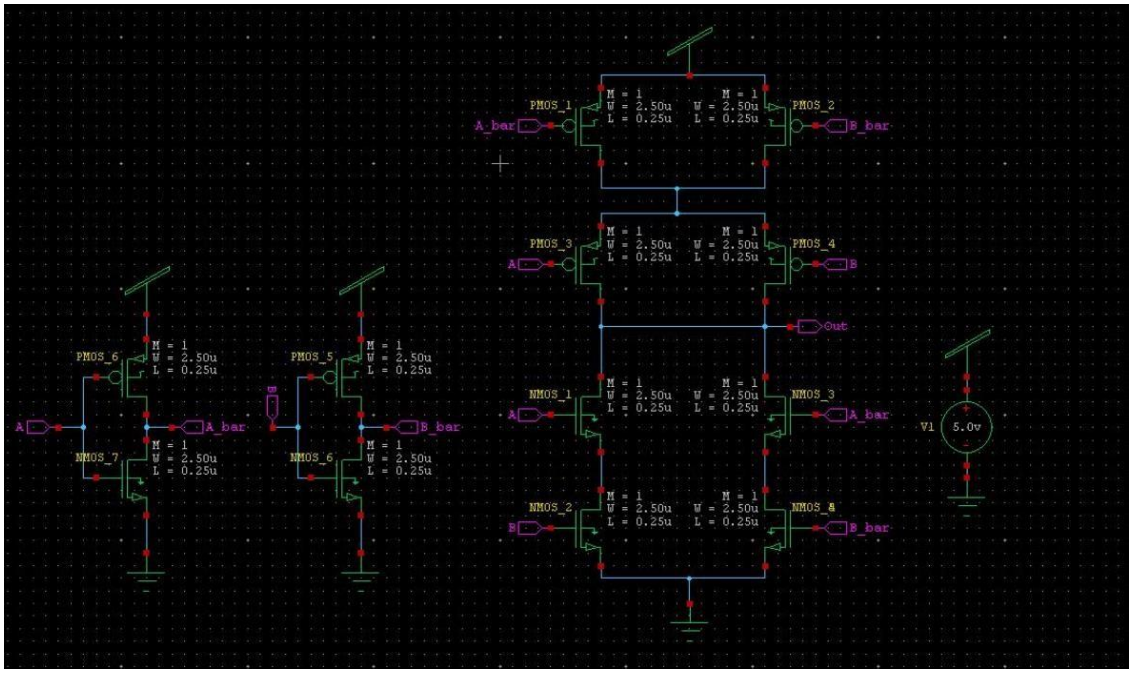
OUTPUT WAVEFORM:



Design of XOR Gate

The **XOR gate** stands for the **Exclusive-OR gate**. The XOR Gate is another type of digital logic gate commonly used in arithmetic operations since it can be used to give the sum of two binary numbers as well as error-detection and correction circuits.

Circuit Diagram:

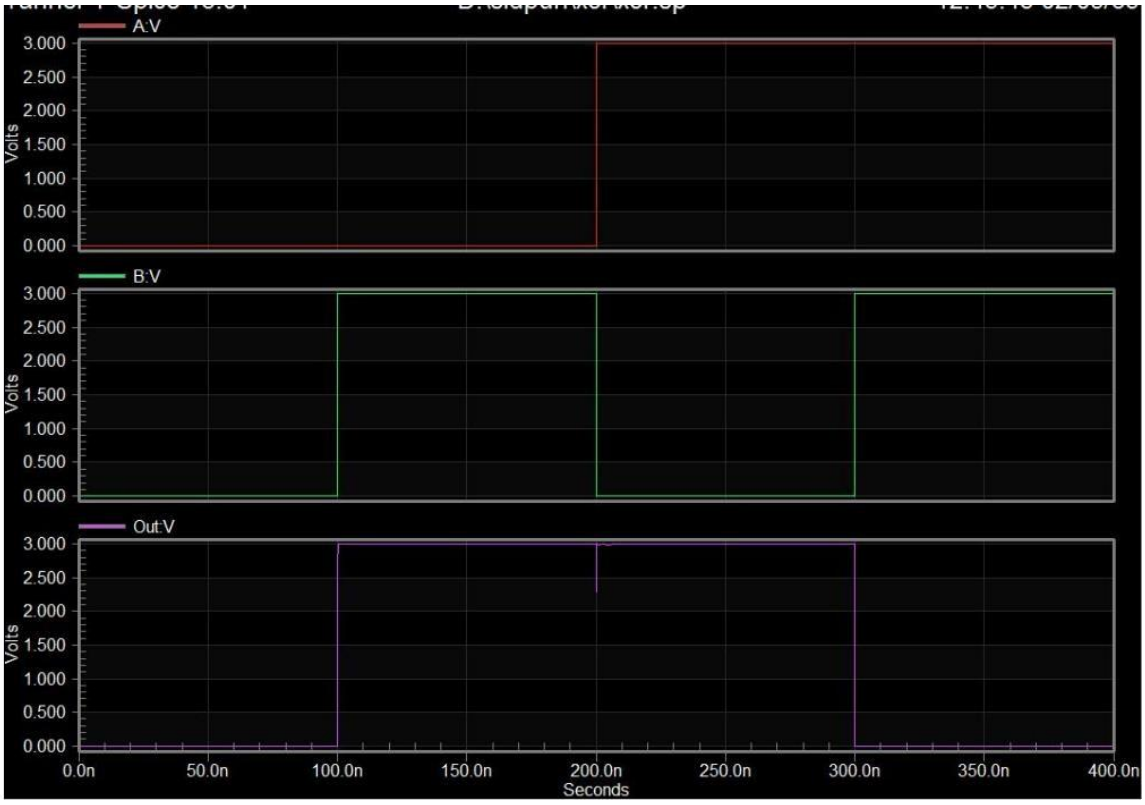


T-Spice Code:

MNMOS_1 Out A N_1 0 NMOS W=450N L=150n AS=2.25p PS=6.8u AD=2.25p PD=6.8u
MNMOS_2 N_1 B Gnd 0 NMOS W=450N L=150n AS=2.25p PS=6.8u AD=2.25p PD=6.8u
MNMOS_3 Out A_bar N_2 0 NMOS W=450N L=150n AS=2.25p PS=6.8u
AD=2.25pPD=6.8u MNMOS_4 N_2 B_bar Gnd 0 NMOS W=450N L=150n AS=2.25p
PS=6.8u AD=2.25pPD=6.8u MNMOS_5 N_2 B_bar Gnd 0 NMOS W=450N L=150n
AS=2.25p PS=6.8u AD=2.25pPD=6.8u MNMOS_6 B_bar B Gnd 0 NMOS W=450N L=150n
AS=2.25p PS=6.8u AD=2.25pPD=6.8u
MNMOS_7 A_bar A Gnd 0 NMOS W=450N L=150n AS=2.25p PS=6.8u AD=2.25pPD=6.8u
MPMOS_1 N_3 A_bar Vdd Vdd PMOS W=900N L=250n AS=2.25p PS=6.8u
AD=2.25pPD=6.8u MPMOS_2 N_3 B_bar Vdd Vdd PMOSW=900N L=250n AS=2.25p
PS=6.8u AD=2.25pPD=6.8u MPMOS_3 Out A N_3 Vdd PMOS W=900N L=250n AS=2.25p
PS=6.8u AD=2.25pPD=6.8u
MPMOS_4 Out B N_3 Vdd PMOS W=900N L=250n AS=2.25p PS=6.8u AD=2.25pPD=6.8u
MPMOS_5 B_bar Vdd Vdd PMOSW=900N L=250n AS=2.25p PS=6.8u AD=2.25pPD=6.8u
22

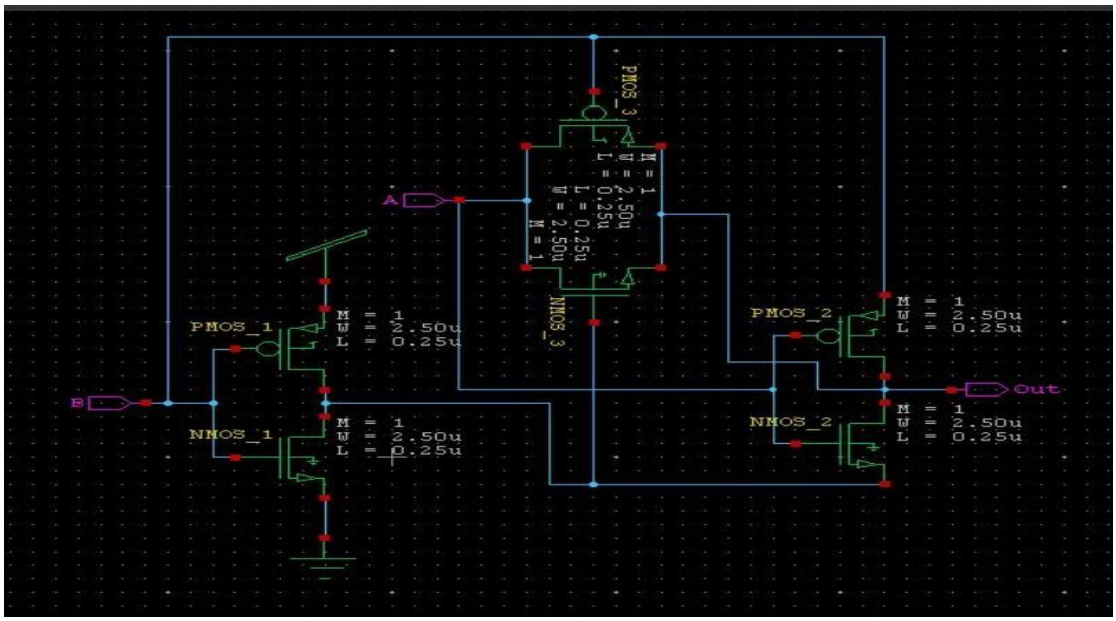
MPMOS_6 A_bar A Vdd Vdd PMOS W=900N L=250n AS=2.25p PS=6.8u
AD=2.25pPD=6.8u
VV1 Vdd Gnd DC 3
V1 A Gnd BIT ({0011} lt=100n ht=100n on=3 off=0 rt=0.1n ft=0.1n)
V2 B Gnd BIT ({0101} lt=100n ht=100n on=3 off=0 rt=0.1n ft=0.1n)
.include "C:\Users\user1\Desktop\dual.md"
.tran 1n 400n
.print V(A) V(B) V (Out)
.end

OUTPUT WAVEFORM:



Design of XOR Gate using Transmission Gate

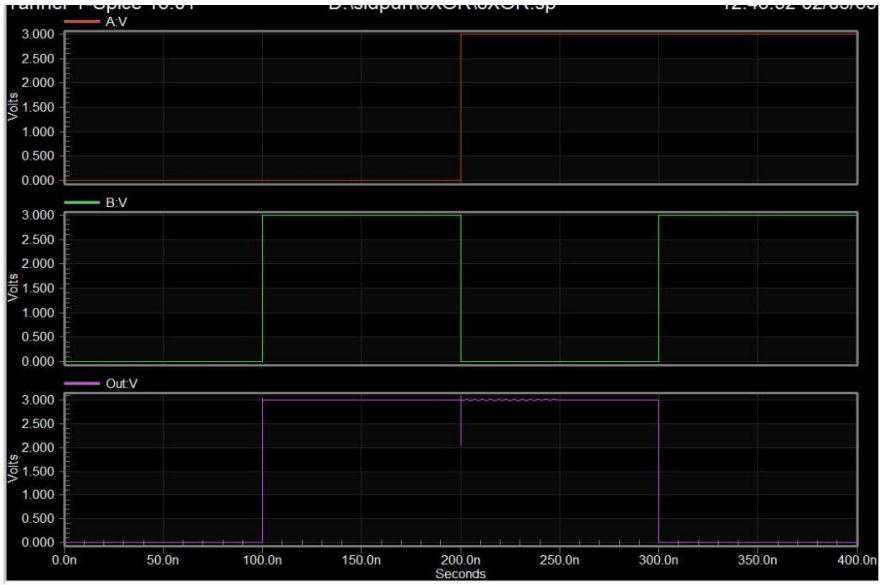
Circuit Diagram:



T-Spice Code:

```
MNMOS_1 N_2 B Gnd 0 NMOS W=450N L=150n AS=2.25p PS=6.8u AD=2.25p PD=6.8u
MNMOS_2 Out A N_2 0 NMOS W=450N L=150n AS=2.25p PS=6.8u AD=2.25p PD=6.8u
MNMOS_3 A N_2 Out 0 NMOS W=450N L=150n AS=2.25p PS=6.8u AD=2.25p PD=6.8u
MPMOS_1 N_2 B Vdd Vdd PMOS W=900N L=150n AS=2.25p PS=6.8u AD=2.25pPD=6.8u
MPMOS_2 Out A B Vdd PMOS W=900N L=150n AS=2.25p PS=6.8u AD=2.25p PD=6.8u
MPMOS_3 A B Out Vdd PMOS W=900N L=150n AS=2.25p PS=6.8u AD=2.25p PD=6.8u
V1 A Gnd BIT ({0011} lt=100n ht=100n on=3 off=0 rt=0.1n ft=0.1n)
V2 B Gnd BIT ({1010} lt=100n ht=100n on=3 off=0 rt=0.1n ft=0.1n)
Vdd Vdd Gnd 3
 .include "C:\Users\user1\Desktop\dual.md"
 .tran 1n 400n
.print V(A) V(B) V (Out)
 .end
```

OUTPUT WAVEFORM:



Design of Buffer circuit using .subckt command

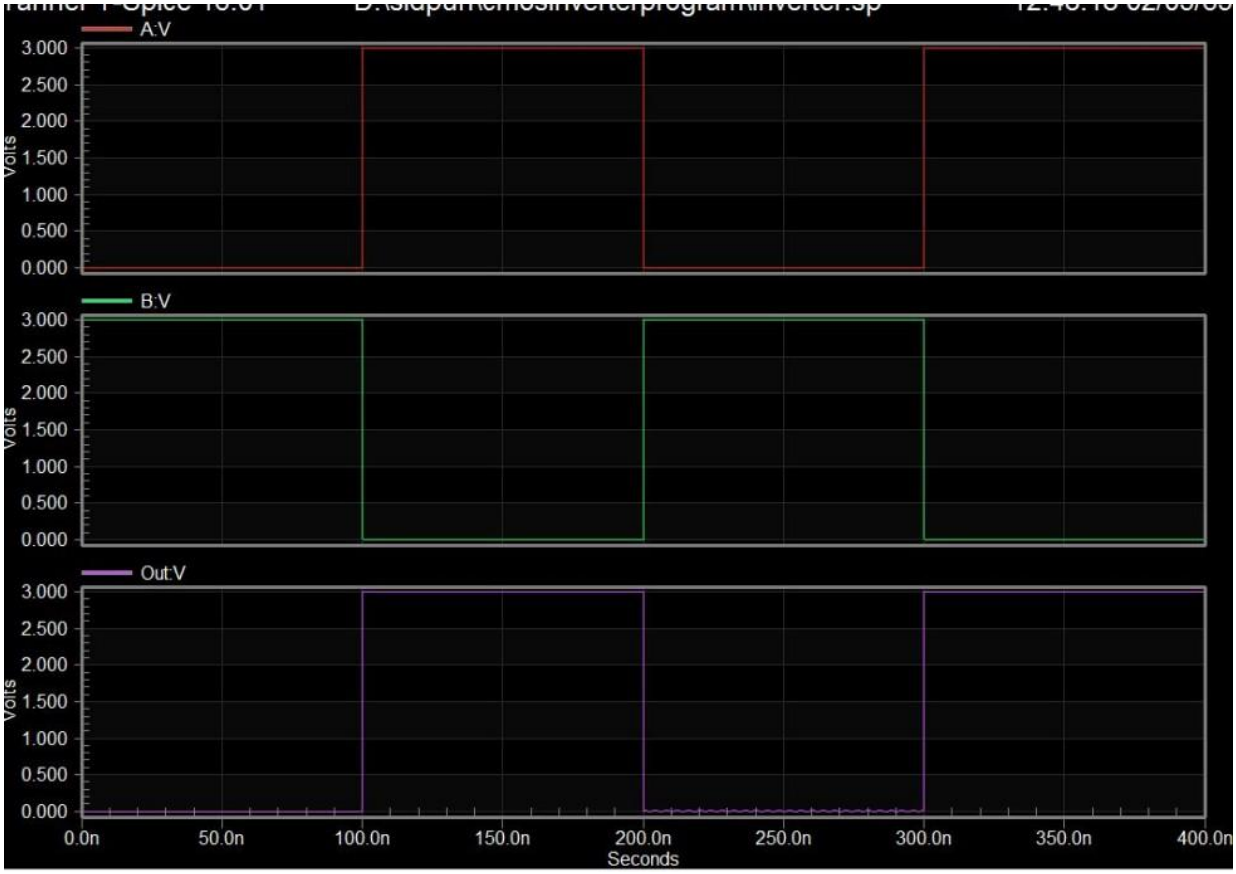
T-Spice Code:

```
.subckt inv In Out Vdd Gnd
MNMOS_1 Out In Gnd 0 NMOS W=450u L=150n AS=2.25p PS=6.8u AD=2.25p PD=6.8u
MPMOS_1 Out In Vdd Vdd PMOS W=900u L=150n AS=2.25p PS=6.8u AD=2.25pPD=6.8u
.ends

 xinv1 A B Vdd Gnd inv
 xinv2 B Out Vdd Gnd inv

Vdd Vdd Gnd 3
 .include "C:\Users\user1\Desktop\dual.md"
 .tran 1n 400n
.print V(A) V(B) V (Out)
.end
```

OUTPUT WAVEFORM:



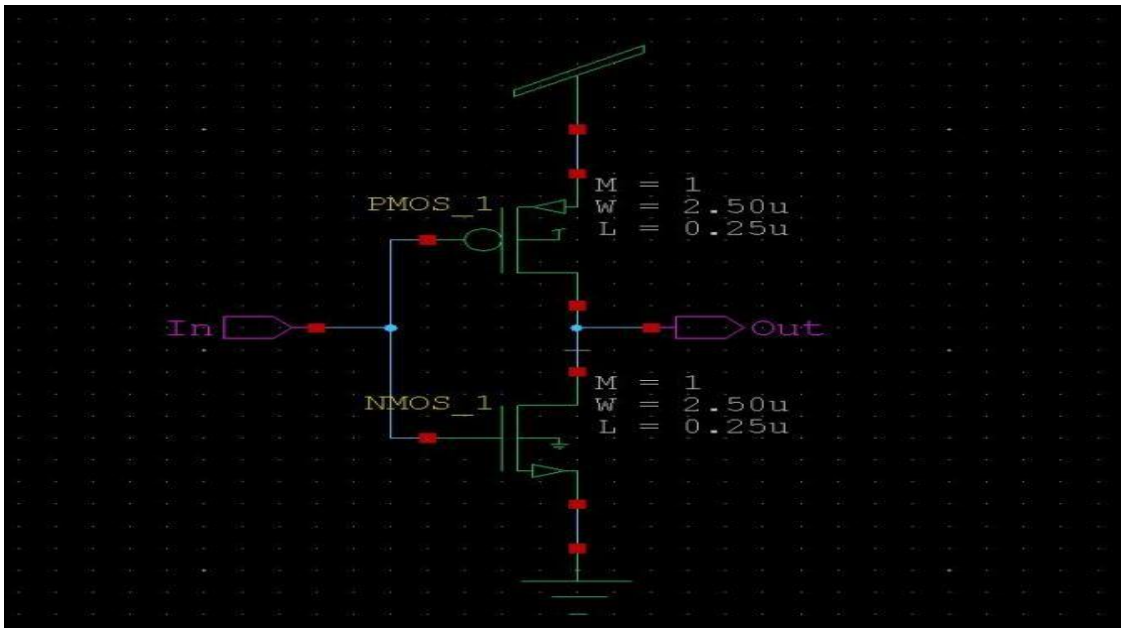
EDA : ANALOG CONTENTS

Serial no.	Topic	Page no.
1.	**Design and analysis of CMOS Inverter.**	
2.	**Design and DC analysis of Resistive load CMOS Inverter.**	
3.	**Design and DC analysis of Capacitive load CMOS Inverter.**	
4.	**Design and analysis of Current Mirror Circuit.**	
5.	**Design and analysis of Differential Amplifier.**	
6.	**Design and analysis of LC Voltage Controlled Oscillator.**	

TITLE:**Design and analysis of CMOS Inverter**

THEORY: :The inverter is truly the nucleus of all digital designs. Once its operation and properties are clearly understood, designing more intricate structures such as NAND gates, adders, multipliers, and microprocessors is greatly simplified. An inverter circuit outputs a voltage representing the opposite logic level to its input. Its primary function is to invert the input signal. That is to say, if the input is low, the output turns high and vice versa. This is the working principle of CMOS inverters.

Circuit Diagram:



T-Spice Code:

```
MNMOS_1 Out In Gnd 0 NMOS W=450n L=150n AS=2.25p PS=6.8u AD=2.25u PD=6.8u
MPMOS_1 Out In Vdd Vdd PMOS W=900n L=150n AS=2.25p PS=6.8u AD=2.25uPD=6.8u
Vdd Vdd Gnd 1 V1 In Gnd 1

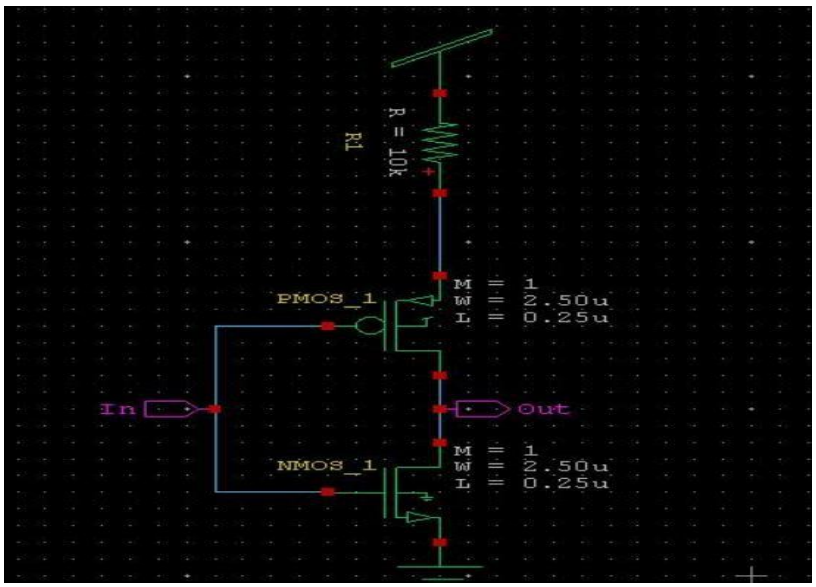
 .include “C:\Users\user1\Desktop\dual.md”
.dc V1 0 1 0.001
 .print V(In) V(Out)
 .end
```

OUTPUT WAVEFORM:



TITLE:**Design and DC analysis of Resistive load CMOS Inverter**

Circuit Diagram:



T-Spice Code:

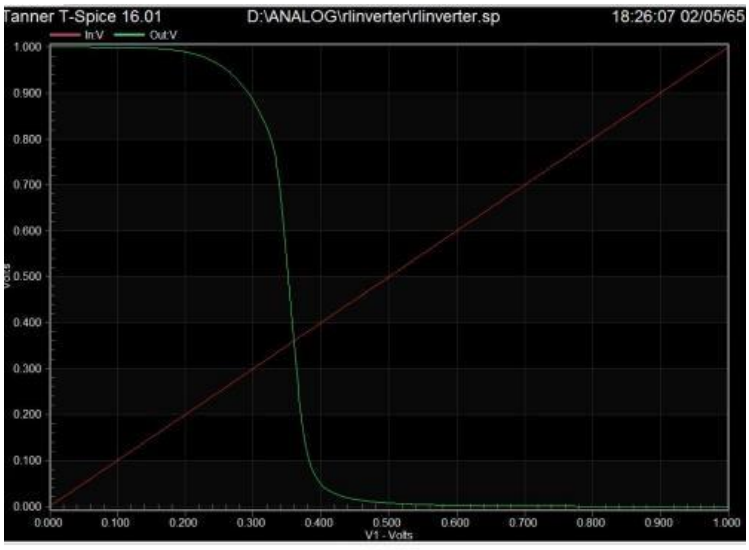
```
RR1 N_1 Vdd R=10k
MNMOS_1 Out In Gnd 0 NMOS W=450n L=150n AS=2.25p PS=6.8u AD=2.25u PD=6.8u
MPMOS_1 Out In Vdd Vdd PMOS W=900n L=150n AS=2.25p PS=6.8u AD=2.25uPD=6.8u
Vdd Vdd Gnd 1 V1 In Gnd 1
```

```
.include “C:\Users\user1\Desktop\dual.md”
.dc V1 0 1 0.001
.print V(In) V(Out)
.end
```

OUTPUT WAVEFORM:



(a)

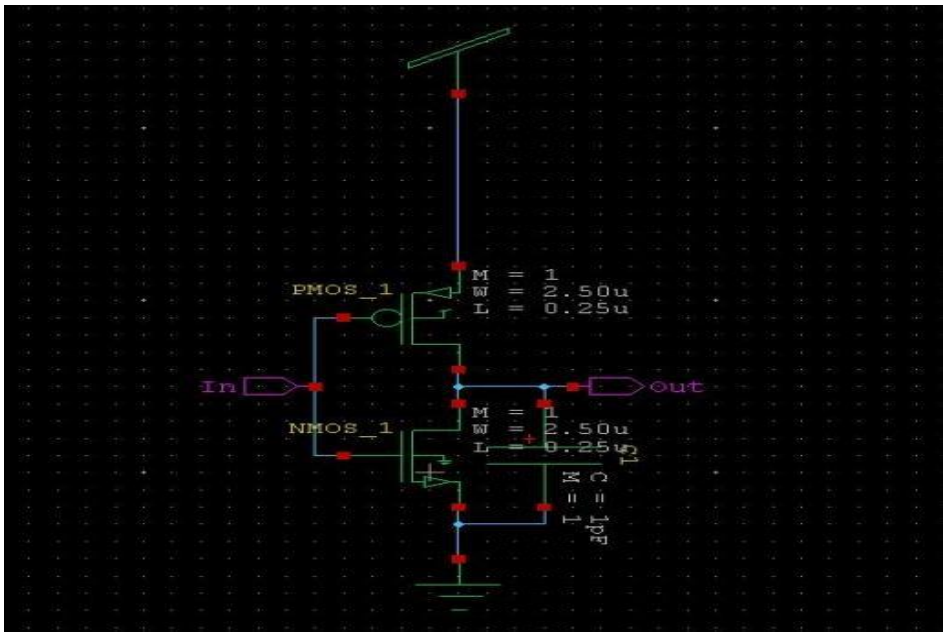


(b)

NOTE: The difference in plots of (a) and (b) is due to a change in Load ResistanceR1, where R1a < R1b.

TITLE:**Design and DC analysis of Capacitive load CMOS Inverter**

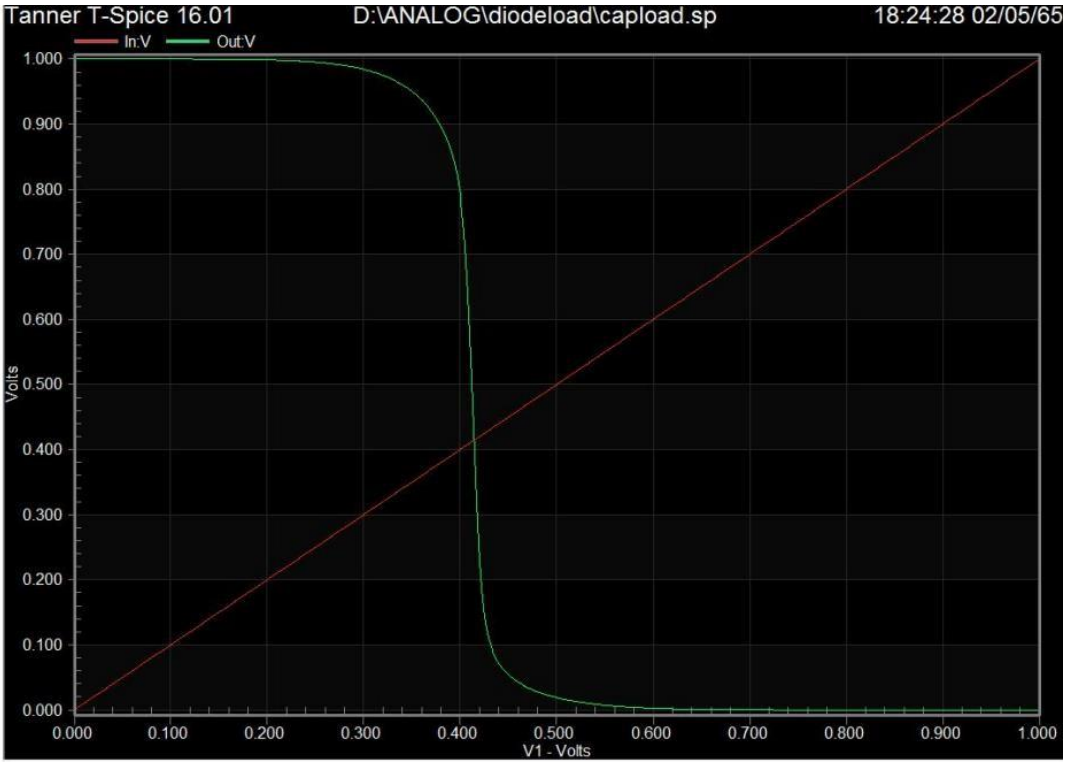
Circuit Diagram:



T-Spice Code:

```
CC1 Out Gnd 2p
MNMOS_1 Out In Gnd 0 NMOS W=450n L=150n AS=2.25p PS=6.8u AD=2.25u
PD=6.8u
MPMOS_1 Out In Vdd Vdd PMOS W=900n L=150n AS=2.25p PS=6.8u
AD=2.25uPD=6.8u
Vdd Vdd Gnd 1
V1 In Gnd 1
 .include “C:\Users\user1\Desktop\dual.md”
 .dc V1 0 1 0.001
 .print V(In) V(Out)
 .end
```

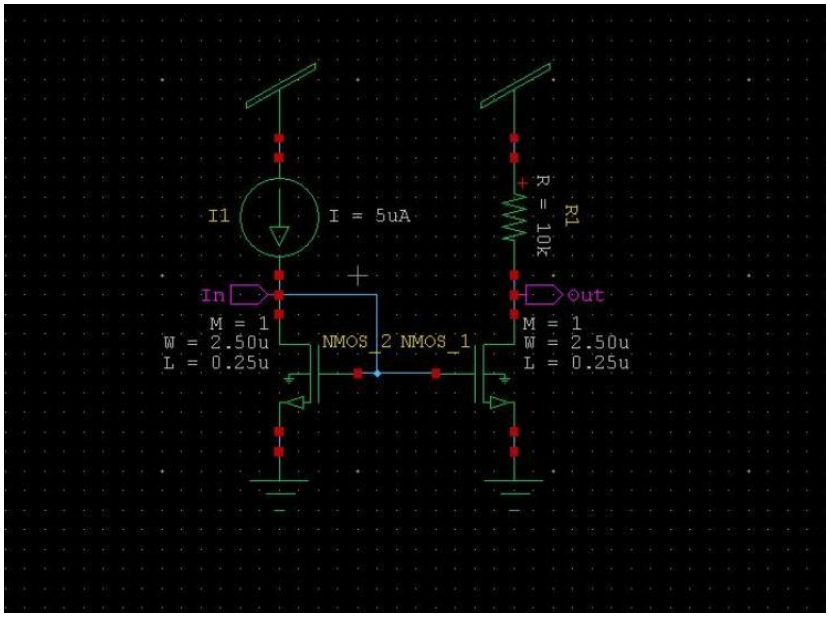
OUTPUT WAVEFORM:



TITLE:**Design and analysis of Current Mirror Circuit**

THEORY: The current mirror is an analog circuit that senses the reference current andgenerates the copy or number of copies of the reference current, with thesamecharacteristics. The replicated current is as stable as the reference current source. Thereplicated current could be the same as the reference current, or it couldbeeithermultiple or fraction of the reference current. Current Mirrors are particularly useful in the integrated circuits, for biasingtheamplifiers. The advantage of biasing the amplifiers with the current source is that itprovides a high voltage gain and good biasing stability.

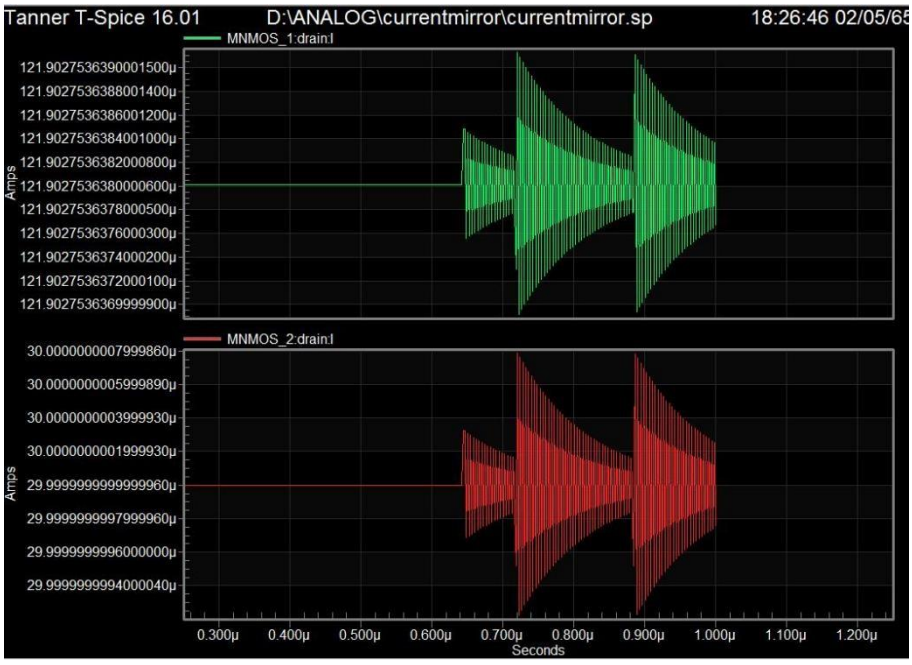
Circuit Diagram:



T-Spice Code:

```
RR1 Vdd Out R=1k
MNMOS_1 Out In Gnd 0 NMOS W=450n L=150n AS=2.25p PS=6.8u AD=2.25u PD=6.8u
MNMOS_1 In In Gnd 0 NMOS W=450n L=150n AS=2.25p PS=6.8u AD=2.25u PD=6.8uII1
 Vdd In DC 30u
Vdd Vdd Gn 5
 .include “C:\Users\user1\Desktop\dual.md”
 .tran 1n 1000n
.print I(MNMOS_2) I(MNMOS_1)
.end
```

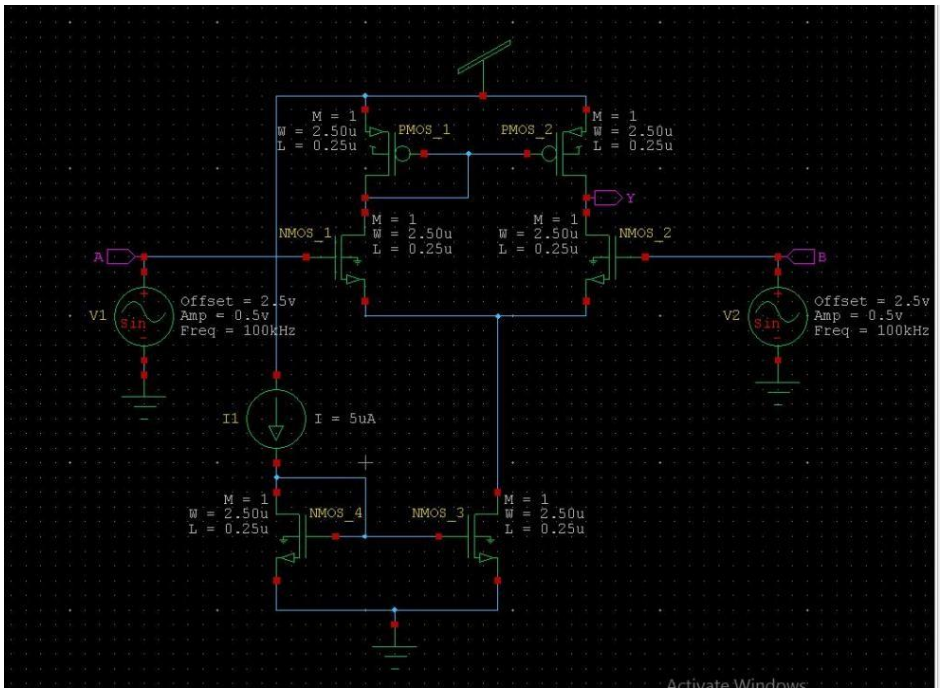
OUTPUT WAVEFORM:



TITLE:**Design and analysis of Differential Amplifier**

THEORY: The differential amplifier is one of the important circuits in analog systemsand circuit designs. It is an electronic amplifier that has two inputs and amplifiesthevoltage difference between those inputs. Here we have constructed one using MOSFETs.

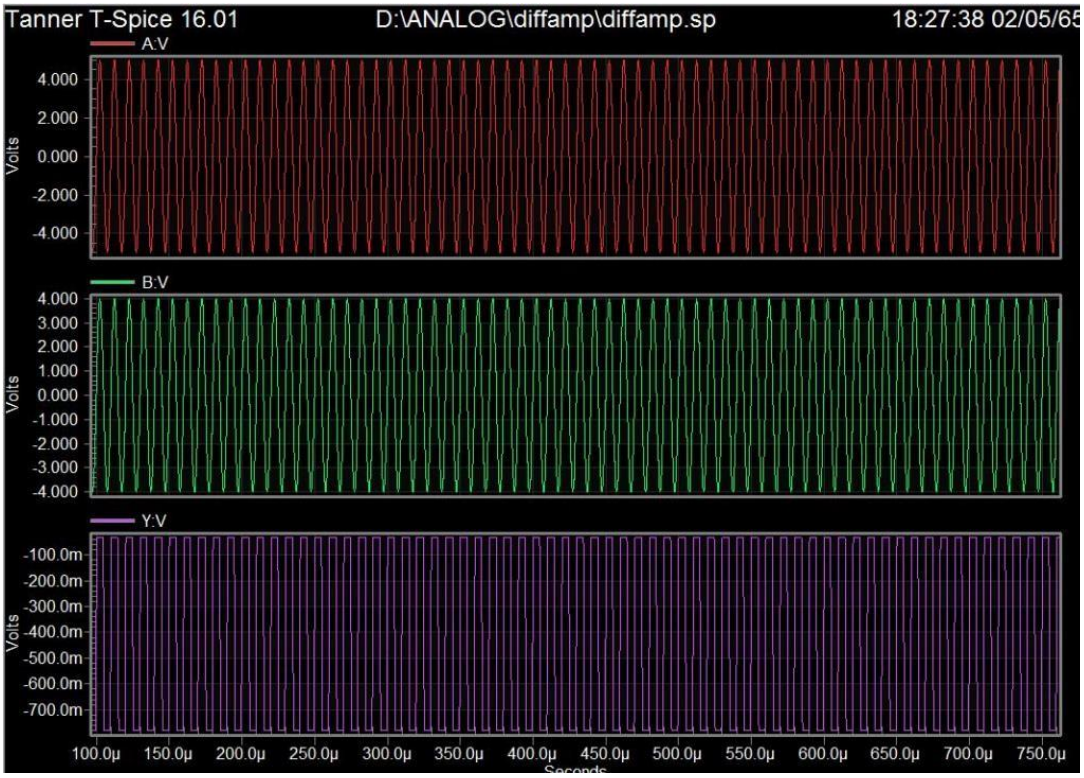
Circuit Diagram:



T-Spice Code:

```
MNMOS_1 N_3 A N_1 0 NMOS W=450n L=150n AS=2.25p PS=6.8u AD=2.25u PD=6.8u
MNMOS_2 Y B N_1 0 NMOS W=450n L=150n AS=2.25p PS=6.8u AD=2.25u PD=6.8u
MNMOS_3 N_1 N_2 Gnd 0 NMOS W=450n L=150n AS=2.25p PS=6.8u AD=2.25uPD=6.8u
MNMOS_4 N_2 N_2 Gnd 0 NMOS W=450n L=150n AS=2.25p PS=6.8u AD=2.25uPD=6.8u
MPMOS_1 N_3 N_3 Vdd Vdd PMOS W=900n L=150n AS=2.25p PS=6.8u
AD=2.25uPD=6.8u MPMOS_2 Y N_3 Vdd Vdd PMOS W=900n L=150n AS=2.25p PS=6.8u
AD=2.25uPD=6.8u
VV1 A Gnd SIN(0 5 100k 0 0 0)
VV2 B Gnd SIN(0 4 100k 0 0 0)
 II1 Vdd N_2 DC 5u
Vss Vss Gnd -5 12
.include “C:\Users\user1\Desktop\dual.md”
 .tran 1n 1m
.print V(A) V(B) V(Y)
.end
```

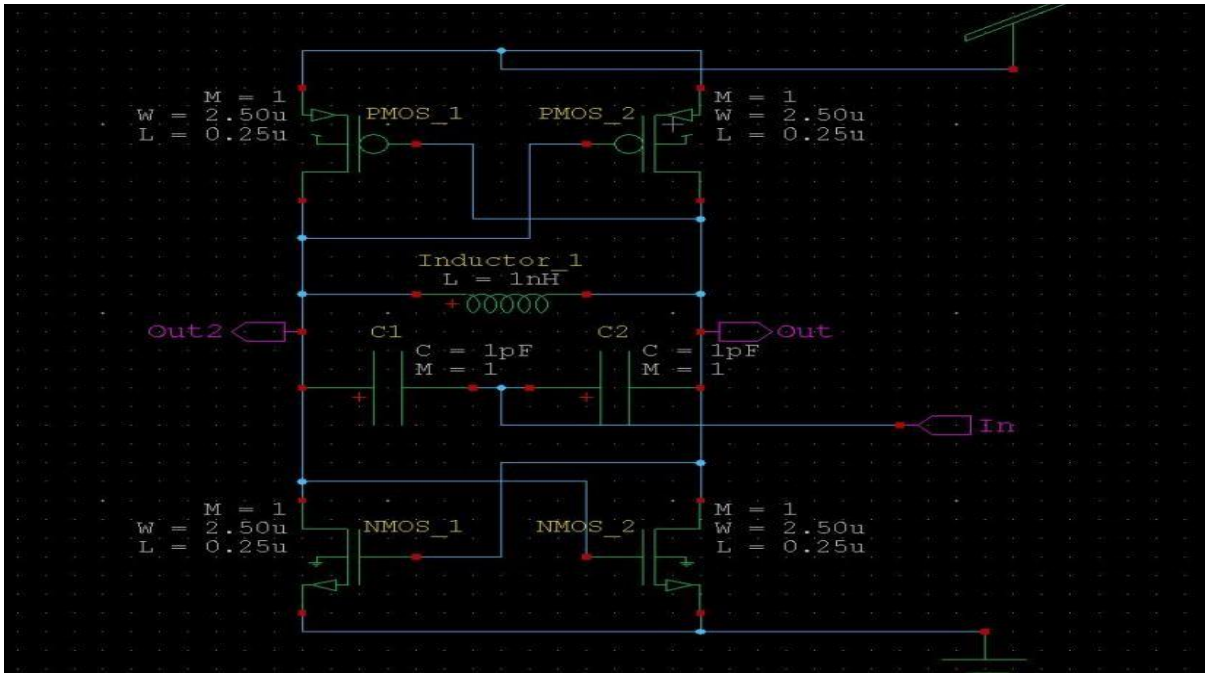
OUTPUT WAVEFORM:



TITLE:**Design and analysis of LC Voltage Controlled Oscilllator**

THEORY: A voltage-controlled oscillator is an oscillator with an output signal whoseoutput can be varied over a range, which is controlled by the input DC voltage. It isanoscillator whose output frequency is directly related to the voltage at its input. Theoscillation frequency varies from a few hertz to hundreds of GHz. By varying theinputDC voltage, the output frequency of the signal produced is adjusted.

Circuit Diagram:

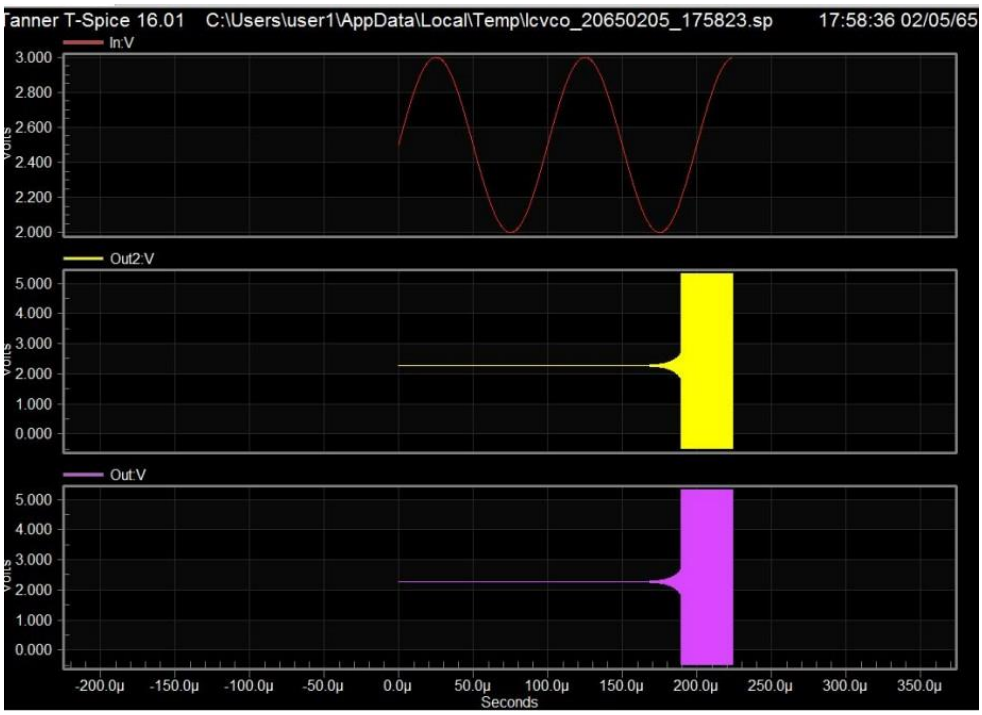


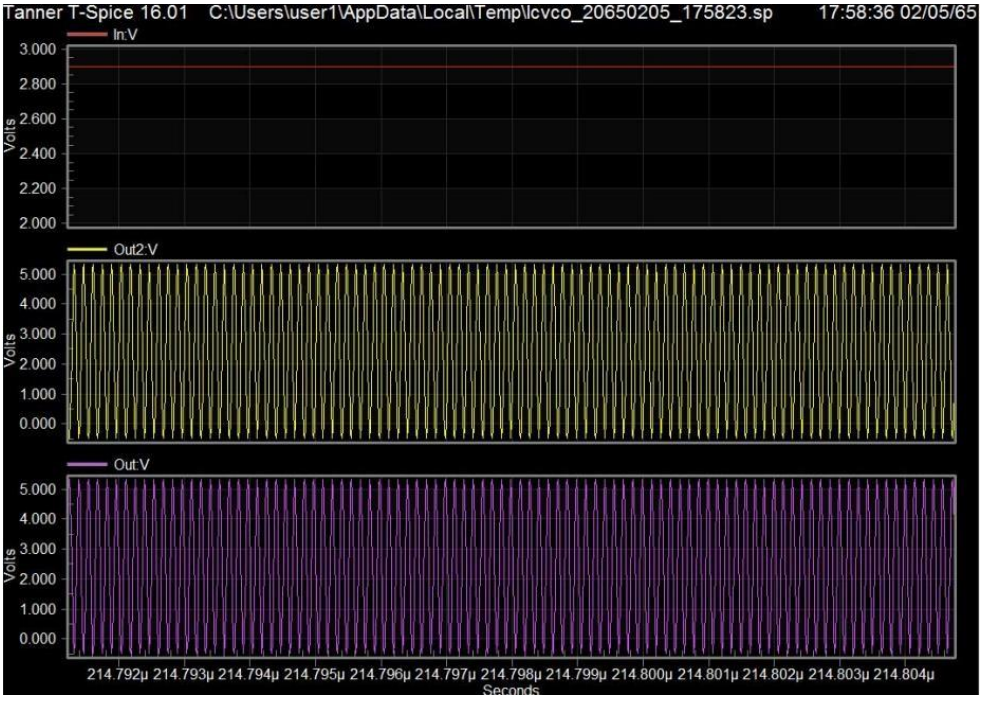
T-Spice Code:

```
CC1 Out 2 In 1p
CC2 In Out 1p
 LInductor_1 Out2 Out L=1n
MNMOS_1 Out2 Out Gnd 0 NMOS W=450n L=150n AS=2.25p PS=6.8u AD=2.25uPD=6.8u
MNMOS_2 Out Out2 Gnd 0 NMOS W=450n L=150n AS=2.25p PS=6.8u AD=2.25uPD=6.8u
MPMOS_1 Out2 Out Vdd Vdd PMOS W=900n L=150n AS=2.25p PS=6.8u
AD=2.25uPD=6.8u MPMOS_2 Out Out2 Vdd Vdd PMOS W=900n L=150n AS=2.25p
PS=6.8u AD=2.25uPD=6.8u
Vdd Vdd Gnd 5 14
VV1 In Gnd SIN(2.5 500m 10k)
 .include “C:\Users\user1\Desktop\dual.md”
```

.tran 1n 1m
.print V(In) V(Out2) V(Out)
.end

OUTPUT WAVEFORM:





CONCLUSION

In this lab we have experienced with analog and digital (Electronic Design Automation) EDA logic circuits by the help of T-SPICE, S-EDIT & W-EDIT and we have observed the waveforms of the logic circuits by the help of this software. The tools work together in a design flow that chip designers use to design and analyze entire semiconductor chips. There is simply no way to manage this level of complexity without sophisticated automation, and EDA provides this critical technology. Without it, it would be impossible to design and manufacture today's semiconductor devices. Since a modern semiconductor chip can have billions of components, EDA tools are essential for them design; this article describes EDA specifically with respect to integrated circuits (ICs).